PAPER NO.
25

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AV-3033N1
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
DANIEL BOULIER
Serial No.: unknown
Filed: unknown
For: ELECTRONIC STILL STORE WITH HIGH SPEED SORTING AND METHOD OF OPERATION

Group Art Unit: 262
Examiner: D. Harvey

PRELIMINARY AMENDMENT

The Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

Please amend the file wrapper continuation application identified above as follows.

In the Specification

At page 1, line 11 after "may" and before "be", delete "than" and substitute --then--.

At page 2, line 25, delete "positioned reduce" and substitute --positioned, reduced--.

At page 5, line 1, delete "referred" and substitute --preferred--. At line 27, delete "fourth" and substitute --forth--.

At page 6, line 4, insert after "22" and before "is" --, which in the preferred embodiment is a random access memory.--. At line 8, after "24" and before "." insert --in the preferred embodiment but which can be any bulk storage memory device in other embodiments--

At page 7, line 9, delete "resolutioncopy" and substitute --resolution copy--. At line 16, delete "usedin" and substitute --used in--. At line 19, delete "continous" and substitute --continuous--.

At page 8, line 7, delete "take" and substitute --taken--. At line 6, after "array" and before "within" insert --as a mosaic which fits--.

In the Drawings

Please approve the drawing change marked on the enclosed sketch.

In the Claims:

Please cancel claim 1.

SUB I 3

2. (Twice Amended) An electronic still store system comprising:

an image store means for [retrievable] retrievably storing therein a plurality of image frame copies of video frames [of video images], the image frame copies comprising data representing a full spatial resolution image [frame copy] and [a] corresponding data representing a reduced spatial resolution image [frame copy] of each frame of video [images] data;

a frame store means which is operable in a first mode [to receive and store] for receiving and storing one of said full spatial resolution images [frame copies] from [the] said image store means and for repetitively [generate] generating a full spatial resolution [output] image [frame] output and operable in a second mode [to receive] for receiving from the image store means and [store] storing a plurality of said reduced spatial resolution images [image frame copies] each at selectively located different positions, the frame store means being further operable in the second mode [to] for repetitively generating [generate a reduced spatial resolution] output

image [frame having an image frame] comprising [a] the stored plurality of said reduced spatial resolution images [image frame copies selectively located at different positions within the output image frame]; and

a size reducer means [coupled to receive] for receiving from the frame store [a] the stored full spatial resolution image [frame copy] and in response thereto [to return] returning to the frame store means a corresponding reduced spatial resolution image [frame copy] and wherein the frame store is operable [to receive and store] for receiving and storing the corresponding reduced spatial resolution image [frame copy] while continuing to store the stored full spatial resolution image [frame copy].

3. (Twice Amended) The electronic still store system according to claim 2 [above], wherein the corresponding reduced spatial resolution image [frame copies] each have a spatial resolution of [one-forth] one-fourth the spatial resolution of the corresponding full spatial resolution image [frame copies in each dimension].

4. (Twice Amended) The electronic still store system according to claim 2 [above], [further comprising] wherein said frame store means includes a central processing unit, controlled by an operator, coupled and operable in said first mode to select which of said [image frame copies] full spatial resolution images stored in said image store means are to be retrieved from the image store means and coupled and operable in said second mode to select which of said reduced spatial resolution images stored in said image store means are to be retrieved and stored in said frame store means and to select the [location] different positions within the frame store means at which each of

said retrieved [image frame copies] reduced spatial resolution images is stored.

Please cancel claim 5.

6. (Twice Amended) The electronic still store system according to claim [5 above] 1, wherein said frame store means further [comprising] comprises an output digital-to-analog converter coupled to receive [said] output image data [frames] from the [the] frame store means and in response thereto to generate an analog video signal representing ~~the received~~ an output image [frames]; and

a monitor coupled to receive the analog video signal and display the output image [frames] represented thereby.

7. (Twice Amended) The electronic still store system according to claim 6 [above], further comprising a video input means for generating an input analog video signal representing [a sequence of] an input video image [frames] and an analog-to-digital converter coupled between the video input means and the frame[s] store means [and] for converting the input analog video signal to a digital form [in which] such that digital data representing said input video image ~~frame~~ [can be] is received and stored by the frame store means.

Please cancel claims 8 through 14.

15. (Amended) A video still store system comprising:

a size reducer coupled to receive a full size image data set representing a full size image frame and to produce a reduced size image data set representing a corresponding reduced size image frame in response thereto;

an image store for storing a plurality of said full size image data sets representing a plurality of full size image frames and for storing a plurality of corresponding reduced size image data sets representing a plurality of reduced size image frames, each of said reduced size image data sets corresponding to one of said full size image data sets; and

a frame store means coupled to selectively receive from either an external source or said image store and store one of said full size image data sets, said frame store [is] being operable such that when a full size image data set is received from an external source or is received from said image store and said image store does not contain a corresponding reduced size image data set, said frame store outputs a copy of said full size image data set to said size reducer and [in response thereto] receives a corresponding reduced size image data set which is outputted to said image store for storage with the corresponding full size image data set.

Please add new claims 16-28.

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16. An apparatus for storing video images as pixel data comprising:

means for receiving and storing in a first memory pixel data representing video images having a first resolution, and for generating from said pixel data representing said video image at said first resolution pixel data representing a corresponding image having a second, lower resolution and for storing said second resolution image data with said first resolution image data in a second memory; and

means for selectively accessing either said data for the image at its first resolution or only the

corresponding image data at said second resolution for any image stored in said bulk storage memory for further processing.

17. The apparatus of claim 16 wherein said means for selectively accessing allows access to a plurality of images at said second resolution and storage of them in selected blocks of memory in said first memory so that they may be further processed as a mosaic of reduced size images.

18. An apparatus for storing video pixel data representing video images of a first resolution and, for each image at a first resolution a corresponding video image at a second resolution comprising:

random access memory means for storing video pixel data representing a full size image at said first resolution and a corresponding reduced size version thereof at a second resolution;

means for storing one at a time in said random access memory means a plurality of said full size images;

memory means for receiving video pixel data from said random access memory means and for storing said full size images and the corresponding reduced size images received from said random access memory means and for outputting, upon a user's command, a selected full size image or only the corresponding reduced size image for the selected full size image for storage in said random access memory means;

means for generating said corresponding reduced size image from any said full size image in said random access memory means to be transferred to said memory means and for storing the video pixel data representing said reduced size image in said random access memory means prior to

storage of the contents of said random access memory means in said memory means.

19. An apparatus for storing video data as full size image and reduced size image of pixel data comprising:

random access memory means for storing video pixel data presented at an input port and having at least one output port;

means for storing video pixel data representing a full size video image at a first resolution in a first group of memory locations in said random access memory means;

bulk storage memory for storing video pixel data and for presenting selected blocks of video data at said input port for storage by said random access memory;

size reducing means coupled to said random access memory means for accessing said image video pixel data stored in said random access memory representing said full size image at said first resolution, and for reducing said image to a reduced size counterpart image at a second, lower resolution and for storing said reduced size image at said second resolution in said random access memory in a second group of storage locations therein; and

control means coupled to said random access memory means, said bulk storage means and to said size reducing means for causing said size reducing means to generate said reduced size image at said second resolution and to store same in said random access memory means in said second group of storage locations each time the video pixel data from said random access memory means is to be transferred to said bulk storage means for storage, and for causing the video pixel data from both said first and second plurality of memory locations in said random access memory means to be transferred to said bulk storage means for storage after said reduced size image is generated and

stored in said second group of storage locations, and for causing selective transfer of video pixel data from said bulk storage means into said random access memory means for storage such that either said first resolution image or only the reduced size second resolution counterpart are transferred into said random access memory means.

20. The apparatus of claim 19 wherein said control means also is coupled for causing selective transfer of said second resolution image directly from said size reducing means into said bulk storage means.

21. The apparatus of claim 19 wherein said control means also is coupled for controlling the memory locations in said random access memory means where the video pixel data defining said second resolution image are stored upon transfer from said bulk storage means.

22. The apparatus of claim 21 wherein said size reducing means produces said second resolution image with 1/16th the resolution of said first resolution image and wherein said control means is coupled for causing transfer of said second resolution image into said random access memory for storage at a selected one of 16 predetermined blocks of memory locations.

23. A system for storing and retrieving video data representing video images which are displayed as rasters of vertically distributed horizontal lines, each represented video image normally occupying a raster of selected vertical and horizontal size, the system comprising:

a video image size reducer having an input coupled to receive video data representing a video image

corresponding to a selected raster size and generate therefrom at an output video data representing a reproduction of said video image corresponding to a selected fractional-size of said selected raster size;

a first store having an input for receiving video data for storage and an output for providing video data retrieved from storage, said first store having a capacity for storing video data representing a video image corresponding to of the selected raster size together with video data representing a reproduction of a video image corresponding to the selected fractional-size of said selected raster size;

a second store having an input for receiving video data for storage and an output for providing video data retrieved from storage, said second store having a capacity for storing video data representing a plurality of video images each corresponding to a video frame of the selected raster size and video data representing the reproduction of each video image of selected fractional size of said selected raster size; and

means for selectively transferring from said first store to said second store either said video data representing a video image corresponding to the selected raster size or said video data representing a reproduction of a video image which is the selected fractional size of said selected raster size.

24. A method of storing video pixel data comprising:

receiving data for a full size image at a first resolution and generating therefrom data representing a reduced size reproduction image at a second, lower resolution;

storing both the full size and the reduced size image in a bulk storage medium; and

selectively accessing either the full size or said reduced size image from said bulk storage medium.

25. The method of claim 24 further comprising the steps of storing a plurality of full size images and their reduced size reproduction images and accessing a plurality of selected reduced size images and storing them in selected blocks of storage locations in a random access memory.

SUB I5

26. The method of claim 24 wherein each full size image occupies upon display a raster of selected vertical and horizontal size, and further comprising the steps of storing a plurality of full size images and their reduced size reproduction images and accessing a plurality of selected reduced size images and storing them in a random access memory and outputting the group of stored reduced size reproduction images as a mosaic of reproduction images occupying a raster of the selected vertical and horizontal size.

A16 cont'd

27. A method of storing video pixel data comprising:

receiving and storing in random access memory video pixel data comprising a full size image;

generating therefrom video pixel data representing a reproduction thereof in the form of a reduced size image at a lower resolution from the full size image data and storing the pixel data representing the reduced size image so generated in additional storage locations in said random access memory along with the full size image;

storing both the full size and the reduced size image in bulk storage memory;

selectively transferring either the full size image or the reduced size image from said bulk storage memory means

into said random access memory means for further processing.

28. A video still store system comprising:

an image store for storing full size image data sets representing a plurality of full size images and for storing a plurality of reduced size image data sets representing a plurality of reduced size images, each of said reduced size image data sets corresponding to one of the full size image data sets;

an external source input for receiving from an external source full size image data sets;

a memory for simultaneous storage of one of said full size image data sets and the corresponding one of said reduced size image data sets;

a size reducer means for receiving from said memory the stored one of said full size image data sets, and for producing and returning to said memory the corresponding reduced size image data set;

said memory being coupled and operative to selectively receive from either the external source input or the image store and to store said one of said full size image data sets, and to output as an output image the stored one of said full size image data sets, and to communicate to the size reducer the stored one of said full size image data sets, and to receive from the size reducer and to store the corresponding reduced size image data set, and to provide to the image store both the stored one of said full size image data sets and the corresponding reduced size image data set, and to receive from the image store and to store at different selected locations selected ones of said plurality of reduced size image data sets, and to output as said output image the stored selected ones such that the selected ones are disposed at different locations

within the output image or to receive and store from said image store only a full sized image data set; and

means to retrieve data from said memory and display it on a raster scanned video display.

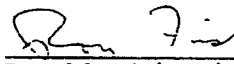
REMARKS

The undersigned thanks the Examiner for the courtesy of the telephone interview conducted during the prosecution of the parent to the above identified case. In response to the discussions therein of new claims written by the undersigned, said new claims are submitted herewith for examination based on the substance of the interview. Further, some of the now pending claims have been retained and amended to eliminate the problems under 35 U.S.C. Section 112 noted in the outstanding office action. New claim 28 is the Examiner's suggested rewrite of claim 9 with some minor changes in terminology and one additional element.

New claims 16 through 28 are in accord with the novelty identified by the Examiner in the first Office Action in the parent of the above identified U.S. patent application. Based upon the content of the Hugh Boyd, Quantel reference, which teaches accessing from disk the entire full size picture before size reduction can occur, these new claims are believed to be allowable. This is so because they teach storing a reduced image with the full size image each time a full sized image is to be stored from the frame buffer to the disk. This allows the user the option of retrieving the entire full size image or only the reduced size counterpart from disk. Mosaics of reduced size counterpart images may be made by accessing several reduced size images and moving them around in the frame buffer. The access time for each reduced size image

is only a fraction of the access time for the entire full size image. This system obviously has a major advantage over the Boyd, Quantel system in that access time for a frame comprised of one or more reduced images will be substantially shorter than the Boyd, Quantel system can provide. This is because the Boyd, Quantel reference does not store a reduced image automatically with the full size counterpart each time a full size image in the frame buffer is to be stored on disk. Thus to access any particular reduced image, the entire full size image must be accessed and loaded into the size reducer. Clearly this takes more time than accessing only the data describing the reduced size image from the disk.

Respectfully submitted,
CIOTTI & MURASHIGE

By 
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PAPER NO. 28

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Norand
5-13-88

In re application of
Daniel A. Beaulier
Serial No.: 018,786
Filed: February 24, 1987
For: ELECTRONIC STILL STORE WITH HIGH SPEED SORTING AND METHOD OF OPERATION

Group Art Unit: 262
Examiner: D. Harvey
Attorney Docket No.: AV-3033 N2

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D. C. 20231. on April 27, 1988

George B. Almeida, Reg. # 20,696 4/27/88
DATE

AMENDMENT

RECEIVED
MAY 11 1988
GROUP 260

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated January 4, 1988, please amend the above-identified application as follows. Applicant includes herewith a Request for an Extension of Time of one month, and authorization for the payment of the requisite fee of $56.00.

IN THE SPECIFICATION:

Page 2, line 11, change "Ditigal" to --Digital--;

Page 4, line 18, before "which" insert --in--; after "which" insert --the sole--;

line 19, delete "1";

line 22, change "FIGURE 1" to --the sole FIGURE--;

Page 5, lines 4-6, change "Apparatus and Method for Chroma Separation, AV-2883, by" to --the U.S. Patent No. 4,675,876, issued September 22,

I cont

I1 concl

1987 to--;;

line 7, before "which" insert --which is assigned

I2 to the same assignee as this application,

and--;

line 18, change "An" to --The--; change "A/D" to --A-D--;

line 28, change "afford" to --affords--;

Page 6, line 7, after "or" insert --from--;

line 21, after "initially" insert a comma --,--;

line 22, after "contain" insert a comma --,--;

line 23, after "resolution" delete the comma --,--; after "image" insert a comma --,--;

Page 7, line 5, after "copy" insert a comma --,--;

line 22, delete "from";

line 25, change "to form" to --, for forming--.

IN THE CLAIMS:

X.1. (thrice amended) An electronic still store system comprising:

an image store means for retrievably storing therein a plurality of image frame copies of video frames, the image frame copies comprising data representing [a] full spatial resolution images [image] and corresponding data representing [a] reduced spatial resolution images [image] of the [each frame of] video frames [data];

I3 cont

[a] frame store means [which is operable in a first mode] for receiving and storing in a first mode one of

said full spatial resolution images from said image store means and for repetitively generating a full spatial resolution image output, and [operable] in a second mode for receiving from the image store means and storing a plurality of said reduced spatial resolution images each at selectively located different positions, the frame store means [being further operable] in the second mode further [for] repetitively generating an image output [image] comprising the stored plurality of said reduced spatial resolution images; and

I 3 cont

[a] size reducer means for receiving from the frame store means the stored full spatial resolution image and in response thereto returning to the frame store means a corresponding reduced spatial resolution image [and], wherein the frame store means receives and stores [is operable for receiving and storing] the returned [corresponding] reduced spatial resolution image while continuing to store the stored full spatial resolution image.

12. (thrice amended) The electronic still store system according to claim 1, wherein the [corresponding] reduced spatial resolution images [image] each have a spatial resolution of one-fourth the spatial resolution of the corresponding full spatial resolution image.

13. (thrice amended) The electronic still store system according to claim 1, wherein said frame store means

I 3 conch

includes a central processing unit, controlled by an operator[, coupled and operable] in said first mode for selecting [to select] which of said full spatial resolution images stored in said image store means is [are] to be retrieved from the image store means, and [coupled and operable] in said second mode for selecting [to select] which of said reduced spatial resolution images stored in said image store means are to be retrieved and stored in said frame store means, and further for selecting [to select] the different positions within a video [the] frame [store means] at which each of said retrieved reduced spatial resolution images is stored.

Claim 6, line 7, change "the received" to --an--.

Claim 7, line 9, delete "frame".

---

6. 15. (twice amended) A video still store system comprising:

I 4 cont

external source means for supplying a full size image data set representing a full size image frame;

a size reducer coupled to receive the [a] full size image data set [representing a full size image frame] for producing therefrom [and to produce] a reduced size image data set representing a corresponding reduced size image frame [in response thereto]:

an image store for storing a plurality of [said] full size image data sets representing a plurality of full size image frames and for storing a plurality of [corresponding] reduced size image data sets representing a plurality of reduced size image frames, each of said reduced size image data sets corresponding to one of said full size image data sets; and

I4 cont

[a] frame store means for storing one of said full size image data sets [coupled to selectively receive] from either the [an] external source or said image store, wherein if [and store one of said full size image data sets, said frame store being operable such that when a full size image data set is received from an external source or is received from said image store and] said image store does not supply [contain] a corresponding reduced size image data set, said frame store outputs a copy of said full size image data set to said size reducer, and receives in turn a corresponding reduced size image data set;

wherein [which is outputted to] said image store stores the reduced size image data set along [for storage] with the previously stored corresponding full size image data set.

16. (amended) An apparatus for storing video images as pixel data comprising:

means for receiving and storing in a first memory pixel data representing a video image [images] having

a first resolution, and for generating from said pixel data representing said video image at said first resolution, pixel data representing a corresponding image having a second[,] lower resolution; [and]

means for storing in a second memory said second lower resolution pixel [image] data together with said first resolution pixel [image] data [in a second memory]; and

means for selectively accessing said first and second memories to supply either said pixel data for the video ~~image at~~ said [its] first resolution, or [only] said pixel data for the corresponding image [data] at said second resolution, [for any image stored in said bulk storage memory] for further processing.

17. (amended) The apparatus of claim 16 wherein said means for selectively accessing allows access to a plurality of sets of pixel data [images] at said second resolution [and storage of them] in selected groups [blocks] of memory locations in said first memory wherein the pixel data at said second resolution simultaneously is [so that they may be further] processed as a single composite mosaic of reduced size images.

18. (amended) An apparatus for storing video pixel data representing video images of a first resolution and, for each of the images [image] at said [a] first

resolution, a corresponding video image at a second resolution comprising:

random access memory means for individually storing video pixel data representing one of a succession of full size images [image] at said first resolution and a corresponding reduced size version thereof at said [a] second resolution;

I4 cont

[means for storing one at a time in said random access memory means a plurality of said full size images;]

memory means for receiving said video pixel data from said random access memory means and for storing said succession of full size images and the corresponding reduced size versions thereof, [images received from said random access memory means] and for outputting upon a user's command, either a selected one of the successive full size images [image] or only the corresponding reduced size versions thereof [image for the selected full size image] for storage back in said random access memory means;

means for selectively generating one of said corresponding reduced size versions [image] from the respective [any said] full size image in said random access memory means, [to be transferred to said memory means] and for transferring [storing] the video pixel data representing said reduced size image to [in said random access memory means prior to storage of] the contents of said memory means via said random access memory means [in said memory means].

19. (amended) An apparatus for storing video pixel data as at least one full size image at a first resolution, and at least one reduced size image thereof at a second lower resolution, [of pixel data] comprising:

random access memory means having an input port and an output port, for storing the video pixel data presented at the [an] input port [and having at least one output port];

[means for storing] said video pixel data representing the [a] full size video image at a first resolution being stored in a first group of memory locations in said random access memory means;

bulk storage memory for also storing the video pixel data and for presenting selected groups [blocks] of video data at said input port for storage by said random access memory means;

size reducing means responsive [coupled] to said random access memory means for directly receiving [accessing] said [image] video pixel data stored in said random access memory means representing said full size image at said first resolution, and for reducing said image to the [a] reduced size [counterpart] image at the [a] second[,] lower resolution, and for supplying [storing] said reduced size image at said second resolution directly back to [in] said random access memory means in a second group of memory [storage] locations therein; [and]

control means coupled to said random access memory means, to said bulk storage memory [means] and to said size reducing means, for causing said size reducing means to generate said reduced size image at said second resolution and to supply [store] same to [in] said random access memory means in said second group of memory [storage] locations; and

said control means further causing the transfer of [each time] the full size and reduced size video pixel data from said random access memory means [is to be transferred] to said bulk storage memory [means] for storage, [and for causing the video pixel data from both said first and second plurality of memory locations in said random access memory means to be transferred to said bulk storage means for storage after said reduced size image is generated and stored in said second group of storage locations,] and for causing the selective transfer [of video pixel data] from said bulk storage memory directly [means] into said random access memory means of [for storage such that] either said full size image at said first resolution [image] or said [only the] reduced size image at said second lower resolution [counterpart are transferred into said random access memory means].

20. (amended) The apparatus of claim 19 wherein said control means also determines the [is coupled for causing] selective transfer of said reduced size image at

said second resolution [image directly] from said size reducing means into said bulk storage memory via the random access memory means.

21. (amended) The apparatus of claim 19 wherein said control means also determines [is coupled for controlling] the memory locations in said random access memory means where the video pixel data defining said reduced size image at said second resolution [image] are stored upon transfer from said bulk storage memory [means].

I4 cont

22. (amended) The apparatus of claim 19 [21] wherein said size reducing means produces said reduced size image at said second resolution [image] with one fourth [1/16th] the spatial resolution of said full size image at said first resolution, [image] and wherein said control means determines the [is coupled for causing] transfer of said reduced size image at said second resolution [image] into said random access memory means for storage at a selected one of 16 predetermined groups [blocks] of said memory locations.

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23. (amended) A system for storing [and retrieving] video data representing video images which are displayable [displayed] as rasters of vertically distributed horizontal lines, each represented video image normally

occupying a raster of selected vertical and horizontal size, the system comprising:

a video image size reducer having an input for receiving [coupled to receive] video data representing a video image corresponding to the [a] selected raster size and for generating [generate therefrom at an output] video data representing a reproduction of said video image at [corresponding to] a selected fractional-size of said selected raster size;

I4 con't

a first store [having an input] for receiving video data for storage and [an output] for providing video data therefrom [retrieved from storage], said first store having a capacity for storing the video data representing a video image corresponding to [of] the selected raster size together with video data representing said [a] reproduction of a video image at [corresponding to] the selected fractional-size [of said selected raster size];

a second store [having an input] for receiving and storing both the video data from the first store [for storage] and [an output] for providing video data therefrom [retrieved from storage], said second store having a capacity for storing video data representing a plurality of video images each corresponding to [a video frame of] the selected raster size, and video data representing a plurality of the reproductions [reproduction] of each video images at the [of] selected fractional-size of said selected raster size; and

means for selectively transferring from said second [first] store to said first [second] store either said video data representing one of the plurality of [a] video images [image] corresponding to the selected raster size, or said video data representing the plurality of reproductions [a reproduction] of each [a] video image, at [which is] the selected fractional-size of said selected raster size.

I4 Cancel

Claims 24, 25, please cancel without prejudice.

26. (amended) The method of claim 29 [24] wherein each one of the full size images [image] occupies upon display a raster of selected vertical and horizontal size, [and] further comprising: [the steps of]

I5 Cont

storing the [a] plurality of full size images and the plurality of their reduced size reproduction images; [and]

retrieving [accessing] the [a] plurality of reproductions of each video image [selected reduced size images]; [and]

storing the plurality of reproductions [them] in a random access memory; and

outputting the [group of] stored plurality of reproductions [reduced size reproduction images] as a mosaic of reproduction images occupying a raster of the selected vertical and horizontal size.

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~~27~~. (amended) A method of storing video pixel data comprising:

receiving and storing in selected storage locations in a random access memory, full video pixel data comprising a full size image;

generating from the full video pixel data, reduced [therefrom] video pixel data representing a reproduction thereof in the form of a reduced size image at a lower resolution; [from the full size image data and]

storing the reduced video pixel data representing the reduced size image [so generated] in additional storage locations in said random access memory along with the full video pixel data [size image];

storing both the full size image and the reduced size image in bulk storage memory; and

selectively transferring either the full size image or the reduced size image from said bulk storage memory [means] into said random access memory [means] for further processing.

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12
~~28~~. (amended) A video still store system comprising:

an external source for supplying a plurality of full size image data sets representative of corresponding full size images;

an image store for storing said full size image data sets [representing a plurality of full size

images], and for storing a like plurality of reduced size image data sets representing a plurality of reduced size images, each of said reduced size image data sets corresponding to one of the full size image data sets;

[an external source input for receiving from an external source full size image data sets;]

a memory for simultaneous storage of one of said full size image data sets and a [the] corresponding one of said reduced size image data sets;

I5 cont

a size reducer means for receiving from said memory the stored one of said full size image data sets, and for producing and returning to said memory the corresponding one of said reduced size image data sets [set];

said memory being responsive [coupled and operative] to [selectively receive from] either the external source [input] or the image store for storing [and to store] said one of said full size image data sets, [and to output as an output image the stored one of said full size image data sets, and to communicate to the size reducer the stored one of said full size image data sets, and to receive from the size reducer and to store the corresponding reduced size image data set,] and for supplying [to provide] to the image store both the stored one of said full size image data sets and the corresponding one of said reduced size image data sets; [set,]

said memory being responsive to [and to receive from] the image store [and] to store at different

selected locations the [selected ones of said] plurality of reduced size image data sets;[, and]

said memory further supplying [to output] as an [said] output image either the plurality of reduced size image data sets arranged [stored selected ones such that the selected one are disposed] at different locations within the output image, or the [to receive and store from said image store only a] full size [sized] image data set; and

means responsive to [retrieve data from] said memory for displaying the output image as [and display it on] a raster scanned video display.

I 5 conch

[Please add the following new Claim 29 to replace original Claims 24, 25.]

SUBJ3

--29. A method of storing video pixel data for access and display comprising:

providing data sets for a plurality of full size images at a first spatial resolution;

generating, from the data sets of the full size images, second data sets representing a corresponding plurality of reduced size reproduction images at a second lower spatial resolution;

storing both the data sets of the plurality of full size images and the data sets of the corresponding plurality of reduced size reproduction images in respective selected groups of storage locations; and

I 6 cont

I 6 concl

selectively accessing either one of the data sets of the plurality of full size images or the sets of the corresponding plurality of the reduced size reproduction images simultaneously.--

REMARKS

By this amendment, Claims 24, 25 are cancelled without prejudice and replaced by new Claim 29; Claims 2-4, 6, 7, 15-23, 26-28 are variously amended and along with Claim 29 are submitted for consideration in view of the remarks following. Applicant notes with appreciation the allowance of Claims 2, 15, 18, 19, 27, 28 if amended to overcome the rejection under 35 USC 112, and the allowance of Claims 3, 4, 6, 7, 20-22 if amended to overcome the 35 USC 112 rejection, and to include the limitations of the base and intervening claims.

In his Office Action, the Examiner rejected Claims 2-4, 6, 7, 15-28 under 35 USC 112, second paragraph; and Claims 16, 17, 23-26 under 35 USC 102(b) as anticipated by Taylor et al, '776.

Applicant has carefully reviewed the specification and has corrected various inconsistencies therein. The claims have also been carefully reviewed particularly in light of the Examiner's rejections and helpful suggestions, and have been amended throughout in keeping with the Examiner's suggestions as well as for purposes of standardizing and/or clarifying the language thereof.

More particularly, regarding the rejection under 35 USC 112, second paragraph, the specific suggestions in Items (paragraphs) 1-6, 8-13, 18-19 and 23-25, of the Office Action, pages 1-4, have been complied with.

In Items 15-17, 21, 29 and 30 the claims in question have been amended to positively recite antecedents for the various terms referred to by the Examiner.

In Item 7, the term "one-fourth" is correct for the term "spatial resolution". One-sixteenth refers to the storage capacity of a single full size image, that is, over a picture raster. (See page 6, lines 15-18). Claim 22 also has been corrected.

In Item 14, lines 23, 24 (of the original claims) the storage refers to both the full size and reduced size data sets as clarified.

In Item 20, lines 13, 14, "either" image (is) stored.

In Item 22, line 2, the means being accessed is now clearly identified.

In Item 26, the passage in lines 9, 10 was deleted as redundant, and the language in lines 5-8 is amended to clarify the storage of full and reduced size image data.

In Items 27, 28, the "video pixel data" and "said succession of full size images" properly refer back to lines 5, 6 and line 6, respectively, of the original claims.

In Items 31 and 32, Claim 25 has been cancelled.

In Item 33, Claim 26 is now made dependent on new Claim 29, and in line 1, "each one of the full size inages" refers back to Claim 29, lines 3-4. In lines 4-5 of original Claim 26, the "reduced size reproduction images" are recited in new Claim 29, line 7.

In Item 34, original Claim 26, line 7, "outputting the stored plurality of..." properly refers back to Claim 29, line 11.

In Item 35, Claims 27 and 28 have been carefully amended to clarify similar problems in antecedents as corrected in the other claims.

In Item 36, Applicant has deleted the term "operable" throughout all the claims and believes the claims as amended herein now recite language which is definite.

Accordingly, Applicant respectfully requests the withdrawal of the rejection under 35 USC 112, second paragraph, of Claims 2-4, 6, 7, 15-28 (and 29).

Regarding now the rejection of Claims 16, 17, 23-26 under 35 USC 102(b) as anticipated by Taylor et al, '776, Applicant has amended Claim 16, and has re-written Claims 24, 25 as new Claim 29. It is submitted that Taylor et al fails to anticipate the features in independent Claims 16 and 29, as well as independent Claim 23.

More particularly, Taylor et al may, in fact, include two stores, or memories 14/24 and 18/20, and an image size changer 23. However there is no further similarity to Applicant's invention as described and claimed.

The electronic arrangement and cooperating functions of the electronics are not similar, and are not the equivalent of the cooperating functions of Applicant's combination, as recited in Claims 16, 17, (new) Claim 29, and Claim 26 dependent upon Claim 29. The size changer 23 of Taylor et al is disposed between his frame store 14/24 and his disc store 18/20, and therefore supplies only reduced (or expanded) images to the disc store 18/20 (contrary to the Examiner's statement that both full and reduced images are stored in the disc store). Taylor et al thus teaches the use of a size change process each time a video image is supplied from the frame store 14/24 to the disc store 18/20 (FIGS. 5. 19), and also when the image is supplied from the disc store back to the frame store (FIGS. 18, 19).

On the other hand, Applicant's size reducer 26 is bidirectionally coupled only to his frame store 22, and is responsive to the frame store to supply a reduced size image at such time as only a full size image is stored in the frame store. In addition, Applicant's frame store 22 then supplies both the full size image and its corresponding reduced size image back to his disc store 24 for storage together. Subsequently, the full size images individually are returned to the frame store 22, or any number of the selected plurality of the reduced size images are returned for storage in the frame store 22, whereupon such re-stored images can be repeatedly read out.

Note further, that in Applicant's system, it is the frame store 22 which is accessed to provide the image output for display, further use, etc. More particularly, the frame store 22 has two modes of access; first, it receives and stores a full size image, which then is repeatedly read out from the frame store 22; or second, it receives and stores all (or part of) a plurality (e.g., 16) of reduced size images, which then are all (or partially) repeatedly read out from the frame store 22 simultaneously as a single mosaic of whatever plurality of reduced size images was stored in the frame store 22. That is, in the second mode, all of the stored, reduced size images are outputted for display simultaneously in a single video picture, each in its assigned two-dimensional location in the picture raster.

Taylor et al fails to provide or intend the above discussed features.

Accordingly, Claim 16 now recites inter alia, means for storing in a second memory (i.e., frame store 22) the second lower resolution pixel data <u>together with a</u> (full) first resolution pixel data, and means for accessing the <u>second</u> memory to supply either the first resolution pixel data (one full video image), <u>or</u> the second resolution pixel data (multiple reduced video images), for further processing. These features are not taught or suggested by Taylor et al.

Claim 17 is dependent upon Claim 16 and further specifies that multiple sets of second resolution pixel data are accessed from selected groups of memory locations in the second memory...to allow simultaneous read out and display of the multiple sets of data at the second resolution in a single composite mosaic. These features also are not taught or suggested by Taylor et al.

Likewise, Claim 29 include steps of providing data sets for a plurality of full size images, generating a like plurality of reduced size images from the respective data sets of full size images, storing both the full size data sets and the reduced size data sets in respective groups of storage locations, and selectively accessing either, one of the full size data sets or (all) of the reduced size data sets simultaneously. Claim 26 further recites steps of storing the plurality of full size images and their reduced size images, in respective groups of storage locations, and retrieving the reduced size images and storing them in a random access memory. The Claim 26 continues with outputting the plurality of reproductions (of the reduced size images) as a full size mosaic, etc.

These features of Claims 29 and 26 are not taught or suggested in Taylor et al.

For the same reasons as above, Claim 23 recites language which is not anticipated by Taylor et al. In Claim 23, a first store stores video data representing a full size video image as well as the reduced size video image

corresponding to the full size video image, a second store receives and stores a plurality of full size video images and a like plurality of the reproductions thereof at a fractional-size. Claim 23 further includes means for transferring either one of the full size video images, or the plurality of reproductions as a full image, from the second store to the first store.

These features also are not taught or suggested in Taylor et al.

Accordingly, Applicant respectfully submits that the rejection of Claims 2-4, 6, 7, 15-28 (and 29) under 35 USC 112, second paragraph, is overcome for reasons given above, and that amended Claims 16, 17, 23-26 are not anticipated by Taylor et al but are allowable thereover as discussed above. Action in the form of allowance of Claims 2-4, 6, 7, 15-23, 26-29 is earnestly solicited.

If Examiner finds slight differences that can be resolved by a telephone interview, Applicant hereby requests leave for such interview by telephoning the undersigned collect at (415) 367-3331.

Respectfully submitted,

AMPEX CORPORATION

By George B. Almeida
George B. Almeida
Agent of Applicant
Registration No. 20,696

Dated: April 27, 1988

401 Broadway, M.S. 3-35
Redwood City, CA 94063-3199

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Daniel A. Beaulier

Serial No.: 018,786

Filed: February 24, 1987

For: ELECTRONIC STILL STORE WITH HIGH SPEED SORTING AND METHOD OF OPERATION

Group Art Unit : 262
Examiner : D. Harvey
Attorney Docket No.: AV-3033 K2

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231. on April 27, 1988

George B. Almeida, Reg. # 20,696

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MAY 11 1988
GROUP 260

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Transmitted herewith is an amendment in the above-identified application.

( ) No additional fee is enclosed because this application was filed prior to October 25, 1965 (effective date of Public Law 89-83).

(X) No additional fee is required.

( ) The fee has been calculated as shown below.

Claims as amended:

	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Additional fee
Total Claims		-			x12	
Independent Claims		-			x34	
Total additional fee for this amendment						

( ) Charge $_____ to Deposit Account No. 01-1771. A duplicate copy of this sheet is enclosed.

(xx) The Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 and 1.17 which may be required by this paper, or credit any overpayment, to Deposit Account No. 01-1771. A duplicate copy of this sheet is enclosed.

Respectfully submitted,
Daniel A. Beaulier
AMPEX CORPORATION

By George B. Almeida
George B. Almeida
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Dated: April 27, 1988
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(REV. 10/7/85)

PAPER NO.
30

AV-3033 N2

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Daniel A. Beaulier

Serial No.: 018,786

Filed: February 24, 1987

For: ELECTRONIC STILL STORE WITH HIGH SPEED SORTING AND METHOD OF OPERATION

Group Art Unit: 262
Examiner: D. Harvey
Attorney Docket No.: AV-3033 N2

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on Oct. 5, 1988

George B. Almeida, Reg. # 20,696 DATE 10/5/88

AMENDMENT UNDER 37 CFR 1.116

RECEIVED
OCT 24 1988
GROUP 260

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated July 22,1988 finally rejecting the claims, and as provided by 37 CFR 1.116, entry of the following amendment as placing the above-identified application in condition for allowance, or in better form for appeal, is respectfully requested.

IN THE CLAIMS

Claims 16, 17 please cancel without prejudice.

7.18. (twice amended) An apparatus for storing video pixel data representing video images of a first resolution and, for each each of the images at said first resolution, a

corresponding video image at a second resolution, comprising:

random access memory means for ~~individually~~ storing video pixel data representing one of a succession of full size images at said first resolution and a corresponding reduced size version thereof at said second resolution;

bulk memory means for receiving said video pixel data from said random access memory means and for storing said succession of full size images and the corresponding reduced size versions thereof, and for outputting upon a user's command, either a selected one of the successive full size images or selected ones of [only] the corresponding reduced size versions thereof for direct transfer to, and storage back in, said random access memory means; and

means responsive to said random access memory means for selectively generating one of said corresponding reduced size versions from the respective full size image in said random access memory means, and for transferring the video pixel data representing ~~said full size image~~ and the corresponding reduced size version back [image] to the contents of said [memory means via said] random access memory means.

Claim 19, line 24, after "resolution" insert

--directly back--;

line 44, after "storage memory" insert

--directly--

Claims 20, 21, please cancel without prejudice.

10. ~~23~~ (twice amended) A system for storing video data representing video images which are displayable as rasters of vertically distributed horizontal lines, each represented video image normally occupying a raster of selected vertical and horizontal size, the system comprising:

a video image size reducer having an input for receiving video data representing a video image corresponding to the selected raster size and for generating video data representing a reproduction of said video image at a selected fractional-size of said selected raster size;

a first store for receiving video data for storage and for providing video data therefrom, said first store having a capacity for storing the video data representing the video image corresponding to the selected raster size simultaneously together with the video data supplied by said video image size reducer representing said reproduction of the video image at the selected fractional-size;

a second store for receiving and storing ~~both~~ the video data ~~from~~ stored in the first store and for providing video data therefrom directly to the first store, said second store ~~having a capacity for~~ further storing video data representing a plurality of additional video images each corresponding to the selected

raster size, and video data representing a plurality of ~~the~~ additional reproductions ~~of each video image~~ at the selected fractional size of said selected raster size; and

means for selectively transferring from said second store directly to said first store either ~~said~~ video data representing of the plurality of video images corresponding to the selected raster size, or ~~said~~ video data representing ~~the~~ all plurality of reproductions ~~of each video image~~ at the selected fractional-size of said selected raster size.

Claim 26, please cancel without prejudice.

~~29~~ 32. (amended) A method of storing video pixel data for access and display comprising:

providing data sets for a plurality of full size images at a first spatial resolution;

generating, from the data sets of the full size images, ~~a~~ second data set[s] representing a corresponding plurality of reduced size reproduction images at a second lower spatial resolution;

storing both the data sets of the plurality of full size images and the data set[s] of the corresponding plurality of reduced size reproduction images in respective selected groups of storage locations; and

selectively accessing [either] from the addressed storage locations a ~~one of the~~ data set representing one of the plurality of full size images, and a data set representing one ~~or the set~~[s] of

the corresponding plurality of the reduced size reproduction images, simultaneously.

Please add the following new Claims 30 and 31 to replace original Claims 20 and 26 respectively.

30. An apparatus for storing video pixel data as at least one full size image at a first resolution, and at least one reduced size image thereof at a second lower resolution, comprising:

random access memory means having an input port and an output port, for storing the video pixel data presented at the input port;

said video pixel data representing the full size video image at a first resolution being stored in a first group of memory locations in said random access memory means;

bulk storage memory for also storing the video pixel data and for presenting selected groups of video data at said input port for storage by said random access memory means;

size reducing means responsive to said random access memory means for receiving said video pixel data stored in said random access memory means representing said full size image at said first resolution, and for ~~reducing~~ producing reduced size video pixel data representing ~~said image to~~ the reduced size image at the second lower resolution, and for supplying said reduced size image at

said second resolution to said random access memory means in a second group of memory locations therein;

control means coupled to said random access memory means, to said bulk storage memory and to said size reducing means, for causing said size reducing means to generate said reduced size image at said second resolution and to supply ~~some~~ said reduced image to said random access memory means in said second group of memory locations;

said control means further causing the transfer of the full size and reduced size video pixel data from said random access memory means to said bulk storage memory for storage, and for causing the selective transfer from said bulk storage memory into said random access memory means of either said full size image at said first resolution or said reduced size image at said second lower resolution; and

wherein said control means also determines the selective transfer of said reduced size image at said second resolution from said size reducing means into said bulk storage memory via the random access memory means.--

--~~31~~ 15. A method of storing video pixel data for access and display comprising:

providing data sets for a plurality of full size image at a first spatial resolution, wherein each one of the full size images occupies upon display a raster of selected vertical and horizontal size;

generating, from the data sets of the full size images, a second data set representing a corresponding plurality of reduced size reproduction images at a second lower spatial resolution;

storing both the data sets of the plurality of full size images and the data set of the corresponding plurality of reduced size reproduction images in respective selected groups of storage locations;

selectively accessing ~~one of the data sets of~~ the plurality of full size images, of the sets of the corresponding plurality of the reduced size reproduction images simultaneously;

wherein the step of accessing further includes, retrieving ~~the~~ plurality of reproductions ~~of each video~~ image, storing the plurality of ~~reproductions~~ in a random access memory, and outputting the stored plurality of ~~reproductions~~ as a mosaic of reproduction images occupying a raster of the selected vertical and horizontal size.--

REMARKS

By this amendment, Claims 16, 17, 20, 21 and 26 are cancelled without prejudice, Claims 18, 19, 23, are variously amended and Claims 20 and 26 are re-written as new Claims 30 and 31, respectively, to make them independent and to include all the limitations of the respective base claim, as suggested by the Examiner. Applicant notes with

appreciation the allowance of Claims 2, 4, 6, 7, 15, 27 and 28 and the indication of allowability of Claims 20 and 26 if re-written.

In his Office Action, the Examiner finally rejected Claims 3, 22, 29 under 35 USC 112, second paragraph, as indefinite; finally rejected Claims 16-19, 21, 23-26 under 35 USC 102(b) as anticipated by Taylor et al; indicated the allowability of Claims 20, 26 if re-written, and allowed Claims 2, 4, 6, 7, 15, 27 and 28.

Regarding the rejection under 35 USC 112, applicant has deleted the word "either" from Claim 29, line 13, and added a comma (,) to line 14, thereby clarifying that the accessing is done to one of the... full size images, or to the reduced size reproduction images in a set simultaneously. Thus the confusion is believed removed.

Regarding the Examiner's indication that the Claims 3 and 22 language of one-fourth the spatial resolution would cause the reduced images also to have one-fourth the size, applicant respectfully refers in particular to page 6, lines 14-18, wherein is stated that ,"Because of the two dimensional nature of a video image, a quarter size image defined by video having one-fourth the spatial resolution of a full size image requires one-sixteenth the storage capacity of a full size, full

spatial resolution image."(See also page 7, lines 10-14). Thus the language in the Claims 3 and 22 is, in fact, correct and definite. One-fourth the spatial resolution refers to each dimension, whereby if a picture (image) is one-fourth the width (horizontally) and one-fourth the height (vertically) it obviously takes up one-sixteenth of the full picture raster. That is, sixteen of the one-fourth resolution images would fit on the raster. Thus, applicant respectfully submits the language of Claims 3 and 22 is definite, and requests that the rejection thereof under 35 USC 112 be withdrawn.

Regarding the rejection of Claims 16-19, 21 and 23-26 under 35 USC 102 (b), applicant respectfully submits that the remaining Claims 18, 19, 23 and 26 (new Claim 31) are not fully met by the cited reference to Taylor et al. For example, Claim 18 recites, inter alia, a random access memory means (frame store 22) for individually storing...succession of full size images...and a corresponding reduced size version thereof at said second resolution (underlining added). Taylor et al fails to describe and does not intend the storage of both a reduced size and a full size image in his frame store (14/24 or 124/125) in the manner of applicant. In fact, any size reduction, and thus reduced size image, is made on the full size image only at the time the latter is transferred from the disk storage (18/20) to the frame store (24/124/125) as

depicted in FIG'S 5, 18 and 19, or from the frame store to the disc storage as depicted in FIG. 19. Applicant's invention on the other hand, as described and claimed, provides image reduction via his size reducer (26) coupled only to the frame store (22), and which receives the full size image only from the frame store whenever there is no reduced size image, and which then returns the reduced size image directly back to the frame store for storage thereof simultaneously with the corresponding full size image.

Contrary to the Examiner's statement in page 3, paragraph 3(a), of his Office Action, Taylor et al does not teach or imply that that his size reducer "does not necessarily provide expansion or reduction," and that "the size reducer may pass the image unchanged." Applicant has carefully reviewed the patent and fails to find therein any such description or implication. In the embodiments which include the size reducer, Taylor et al specifically employs an image size change each time a full size image is transferred between storage devices, and fails to imply that the size reducer may pass the image unchanged. If no size reduction is to be made, Taylor et al specifies merely omitting the size changing processor entirely (Col 5, lines 54-57). In any event, Taylor et al fails to store both the full size image and its reduced size version in his frame store as described and claimed by applicant.

In paragraph 3(b), page 3, of the Office Action, the Examiner notes that Taylor et al provides a size reducer output which is fed back to the frame store (but) via the disc store. Such a configuration fails to anticipate applicant's circuit configuration, wherein the size reducer 26 is directly coupled (only) to the frame store 22. This configuration allows applicant the advantages of high speed transfer of multiple, reduced size images in a single frame of video data. In the configuration of FIG'S 5, 18 or 19, Taylor et al must pass a frame of video data through his size changer 23 prior to supplying his frame store, whereupon he then accesses the frame store. Applicant respectfully submits that Taylor's use of a size changer between the two stores is an integral feature of his system, and that the re-arrangement thereof in the manner of applicant's system is made apparent only through hindsight and by application of the teachings of applicant.

Accordingly, Claims 18, 19 and 23 are variously amended herewith to further clarify the language thereof over the reference to Taylor et al. Claim 18 recites inter alia; a "random access memory means for... storing video pixel data representing... full size images... and a corresponding reduced size version thereof at said second resolution"; bulk memory means which stores both size images and which transfers either size of the images directly back to the random access memory means, with no other circuit

therebetween; and means for generating the reduced images from the full size images and returning both directly back to the contents of the random access memory means. Taylor et al fails to teach the above features of storing both image sizes simultaneously in the random access memory, the direct transfer of images between the disc storage and random access memory, or the transfer of images directly between the size reducer and only the random access memory.

Likewise, Claims 19 and 23 also recite the above features in differing language and terms, and thus are not anticipated by Taylor et al for the same reasons given above.

Claims 20 and 26 have been re-written as new Claims 30 and 31 as suggested by the Examiner, to include the limitations of the respective base claim, and new Claim 31 has been amended to overcome the 112 rejection as discussed above. Accordingly, applicant respectfully submits that claims 3,18,19, 22, 23, 29, 30 and 31, along with (allowed) Claims 2, 4, 6, 7, 15, 27 and 28, are in condition for allowance, which action is earnestly solicited.

If Examiner finds slight differences that can be resolved by a telephone interview, Applicant hereby requests

leave for such interview by telephoning the undersigned collect at (415) 367-3331.

If the Examiner persists in his final rejection of the subject application, applicant respectfully requests entry of the amendments for purposes of appeal.

Respectfully submitted,

AMPEX CORPORATION

By George B. Almeida
George B. Almeida
Agent of Applicant
Registration No. 20,696

Dated: October 5, 1988
401 Broadway, M.S. 3-35
Redwood City, CA 94603-3199

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Daniel A. Beaulier

Serial No.: 018,786 Group No.: 262

Filed: February 24, 1987 Examiner: D. Harvey

For: ELECTRONIC STILL STORE WITH HIGH SPEED SORTING AND METHOD OF OPERATION

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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OCT 24 1988

GROUP 260

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application.

STATUS

2. Applicant is
   - ☐ a small entity — verified statement:
     - ☐ attached.
     - ☐ already filed.
   - ☒ other than a small entity.

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United State Postal Sevice on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

George B. Almeida
(Type or print name of person mailing paper)

Date: 10/5/88

George B. Almeida
(Signature of person mailing paper)

EXTENSION OF TERM

NOTE: **"Extension of Time in Patent Cases (Supplement Amendments) — If a timely and complete response has been filed after a Non-Final Office Action,** *an extension of time is not required to permit filing and/or entry of an additional amendment after expiration of the shortened statutory period.*

If a timely response has been filed after a Final Office Action, *an extension of time is required to permit filing and/or entry of a Notice of Appeal or filing and/or entry of an additional amendment after expiration of the shortened statutory period unless the timely-filed response placed the application in condition for allowance. Of course, if a Notice of Appeal has been filed within the shortened statutory period, the period has ceased to run." Notice of December 10, 1985 (1061 O.G. 34-35).*

NOTE: See 37 CFR 1.645 for extensions of time in interference proceedings and 37 CFR 1.550(c) for extensions of time in reexamination proceedings.

3. The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply

(complete (a) or (b) as applicable)

(a) ☐ Applicant petitions for an extension of time for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$56.00	$28.00
☐	two months	$170.00	$85.00
☐	three months	$390.00	$195.00
☐	four months	$610.00	$305.00

Fee $_____

If an additional extension of time is required please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $ _____

OR

(b) ☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEE FOR CLAIMS

4. The fee for claims has been calculated as shown below:

	(Col. 1) CLAIMS REMAINING AFTER AMENDMENT		(Col. 2) HIGHEST NO PREVIOUSLY PAID FOR	(Col. 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
TOTAL	* 15	MINUS ** 19	= 0	x6=	$		x12=	$	Ø
INDEP.	* 10	MINUS *** 9	= 1	x17=	$		x34=	$	34
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+55=	$		+110=	$	Ø
				TOTAL ADDIT. FEE	$ $	OR	TOTAL	$	34

* If the entry in Col. 1 is less than entry in Col. 2, write "0" in Col. 3.
** If the "Highest No. Previously Paid for" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest No. Previously Paid For" (Total or indep.) is the highest number found in the appropriate box in Col. 1 of a prior amendment or the number of claims originally filed.

(complete (c) or (d) as applicable)

(c) ☐ No additional fee for claims is required

OR

(d) ☒ Total additional fee for claims required $ 34.00

FEE PAYMENT

5. ☐ Attached is a check in the sum of $_____

☐ Charge Account No. 01-1771 the sum of $ 34.00

A duplicate of this transmittal is attached.

FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

6. ☒ If any additional extension and/or fee is required charge Account No. 01-1771

AND/OR

☒ If any additional fee for claims is required, charge Account No. 01-1771

George B Almeida 10/5/88

Reg. No.: 20,696

SIGNATURE OF ATTORNEY

Tel. No.: (415) 367-3331

George B. Almeida

Type or print name of attorney

401 Broadway

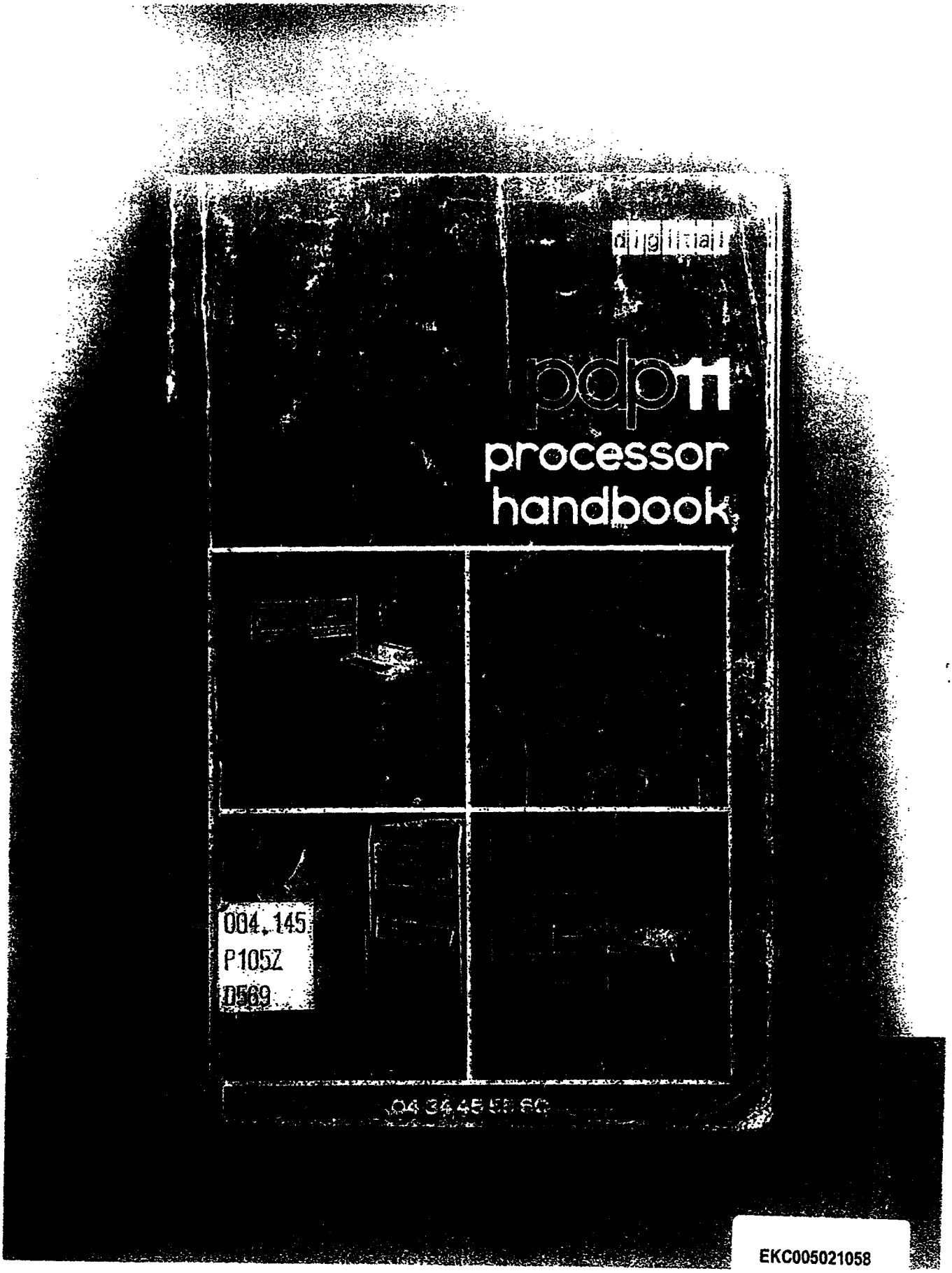
P.O. Address

Redwood City, CA 94063

EXHIBIT 20

Redacted

EXHIBIT 21


digital
pdp11
processor
handbook
004.145
P105Z
D569
EKC005021058

```
;       3) RESTORE REGISTERS
;       4) ISSUE AST EXIT DIRECTIVE
;
BA:     MOV     R0,-(SP)        ;PUSH (SAVE) R0
        MOV     R1,-(SP)        ;PUSH (SAVE) R1
        MOV     R2,-(SP)        ;PUSH (SAVE) R2
```

The position-dependent version of the subroutine contains a relative reference to an absolute symbol ($OTSV) and a literal reference to a relocatable symbol (BA). Both references are bound by the task builder to fixed memory locations. Therefore, the routine will not execute properly as part of a resident library if its location in virtual memory is not the same as the location specified at link time.

In the position-independent version, the reference to $OTSV has been changed to an absolute reference. In addition, the necessary code has been added to compute the virtual location of BA based upon the value of the program counter. In this case, the value is obtained by adding the value of the program counter to the fixed displacement between the current location and the specified symbol. Thus, execution of the modified routine is not affected by its location in the image's virtual address space.

STACKS

The stack is part of the basic design architecture of the PDP-11. It is an area of memory set aside by the programmer or by the operating system for temporary storage and linkage. It is handled on a LIFO (last-in/first-out) basis, where items are retrieved in the reverse of the order in which they were stored. On a PDP-11, a stack starts at the highest location reserved for it and expands linearly downward to a lower address as items are added to the stack.

You do not need to keep track of the actual locations into which data is being stacked. This is done automatically through a stack pointer. To keep track of the last item added to the stack, a general register always contains the memory address when the last item is stored in the stack. In the PDP-11, any register except register 7 (the PC) may be used as a stack pointer under program control; however, instructions associated with subroutine linkage and interrupt service automatically use register 6 as a *hardware* stack pointer. For this reason, R6 is frequently referred to as the system SP. Stacks in the PDP-11 may be maintained in either full word or byte units. This is true for a stack pointed to by any register except R6, which must be organized in full word units only. Byte stacks, Figure 5-1, require instructions capable of operating on bytes rather than full words.

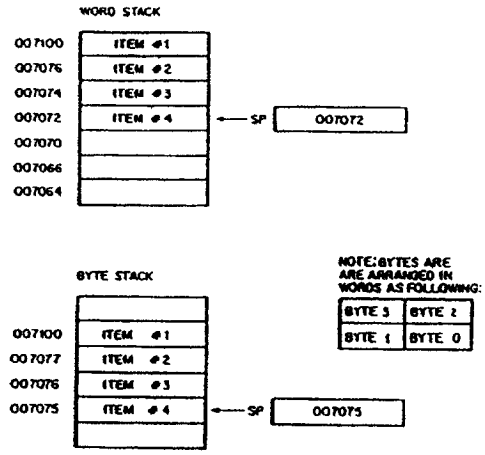


Figure 5-1 Word and Byte Stacks

Items are added to a stack using the autodecrement addressing mode. Adding items to the stack is called PUSHing, and is accomplished by the following instructions:

```
MOV     Source,-(SP)     ;MOV Contents of Source Word
                         ;onto the stack
                                or
MOVB    Source,-(SP)     ;MOVB Source Byte onto
                         ;the stack
```

Data is thus PUSHed onto the stack.

Removing data from the stack is called a POP (popping from the stack). This operation is accomplished using the autoincrement mode:

```
MOV     (SP)+, Destination     ;MOV Destination Word
                               ;off the stack
                                      or
MOVB    (SP)+, Destination     ;MOVB Destination Byte
                               ;off the stack
```

After an item has been popped, its stack location is considered free and available for other use. The stack pointer points to the last used location, implying that the next lower location is free. Thus, a stack may represent a pool of sharable temporary storage locations.

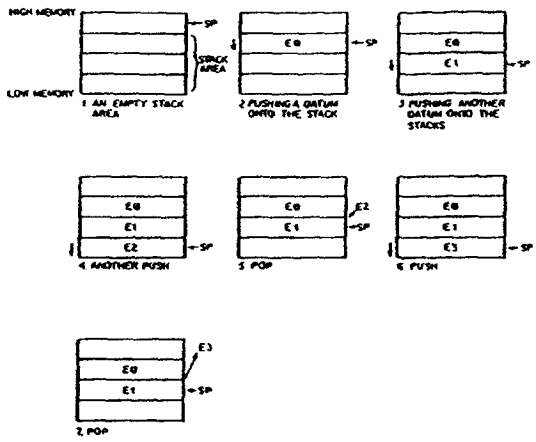


Figure 5-2 Illustration of Push and Pop Operations

Uses for the stack

- Often one of the general purpose registers must be used in a subroutine or interrupt service routine and then returned to its original value. The stack can be used to store the contents of the registers involved.
- The stack is used in storing linkage information between a subroutine and its calling program. The JSR instruction, used in calling a subroutine, requires the specification of a linkage register along with the entry address of the subroutine. The content of this linkage register is stored on the stack, so as not to be lost, and the return address is moved from the PC to the linkage register. This provides a pointer back to the calling program so that successive arguments may be transmitted easily to the subroutine.
- If no arguments need be passed by stacking them after the JSR instruction, the PC may be used as the linkage register. In this case, the result of the JSR is to move the return address in the calling program from the PC onto the stack and replace it with the entry address of the called subroutine.
- In many cases, the operations performed by the subroutine can be applied directly to the data located on or pointed to by a stack without the need ever actually to move the data into the subroutine area.

```
;CALLING PROGRAM
MOV     SP,R1           ;R1 IS USED AS THE STACK
JSR     PC,SUBR         ;POINTER HERE.

;SUBROUTINE
ADD     (R1)+,(R1)      ;ADD ITEM #1 to #2,PLACE
                        ;RESULT IN ITEM #2,
                        ;R1 POINTS TO
                        ;ITEM #2 NOW
```

Because the PDP-11 hardware already uses general purpose register R6 to point to a stack for saving and restoring PC and processor status word (PS) information, it is convenient to use this same stack to save and restore immediate results and to transmit arguments to and from subroutines. Using R6 in this manner permits extreme flexibility in nesting subroutines and interrupt service routines.

Since arguments may be obtained from the stack by using some form of register indexed addressing, it is sometimes useful to save a temporary copy of R6 in some other register which has been saved at the beginning of a subroutine. If R6 is saved in R5 at the beginning of the subroutine, R5 may be used to index the arguments while R6 is free to be incremented and decremented in the course of being used as a stack pointer. If R6 had been used directly as the base for indexing and not "copied," it might be difficult to keep track of the position in the argument list, since the base of the stack would change with every autoincrement/decrement which occurs.

However, if the contents of R6 (SP) are saved in R5 before any arguments are pushed onto the stack, the position relative to R5 would remain constant.

Return from a subroutine also involves the stack, as the return instruction, RTS, must retrieve information stored there by the JSR.

When a subroutine returns, it is necessary to "clean up" the stack by eliminating or skipping over the subroutine arguments. One way this can be done is by insisting that the subroutine keep the number of arguments as its first stack item. Returns from subroutines then involve calculating the amount by which to reset the stack pointer, resetting the stack pointer, then storing the original contents of the register which was used as the copy of the stack pointer.

- Stack storage is used in trap and interrupt linkage. The program counter and the processor status word of the executing program are pushed on the stack.

CONSOLE

The CPU console emulator feature permits control of the PDP-11/04 from any ASCII terminal connected to the processor. Console emulator operations include the normal memory LOAD, EXAMINE, and DEPOSIT, in addition to START or BOOT. This ROM-resident virtual console routine emulates all the functions of a normal programmers' console and provides at the keyboard the equivalent capability of any serial ASCII terminal connected to the system.

The operational programmers' console is a useful aid for program development. The 11/04 includes a maintenance feature which aids in system error diagnostics. When in maintenance mode, the programmers' console enables the CPU's microcode to be single stepped and the UNIBUS addresses and data to be displayed or printed. Detailed information about the operators' and programmers' consoles is presented in the section of this chapter which discusses the PDP-11/34.

Usual Mechanical Conditions

These requirements may vary or be altered according to site conditions; a DIGITAL salesperson can offer appropriate information about any specific situation.

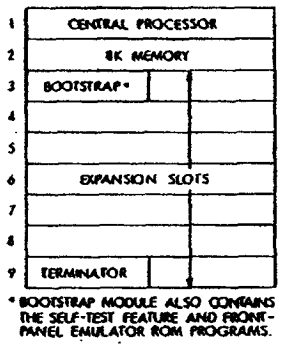


Figure 6-1 PDP-11/04 Backplane

PDP-11/34

The PDP-11/34 is a mid-range member of the PDP-11 family of processors. Features include:

- Integral memory management hardware that provides program protection, memory relocation, and addressing of up to 124K 16-bit words

- Integral extended instruction set (EIS) that provides hardware fixed-point arithmetic in double-precision mode (32-bit operands).
- Self-test diagnostic routines which are automatically executed every time the processor is powered up, the console emulator routine is initiated, or the bootstrap routine is initiated.
- Operator front panel with built-in CPU console emulator that allows control from any ASCII terminal without the need for the conventional front panel with display lights and switches.
- Automatic bootstrap loader which allows system restart from a variety of peripherals devices without manual switch toggling or key-pad operations.
- Choice of 5¼-inch or 10½-inch high mounting chassis.

MEMORY

The PDP-11/34 is available with MOS memory, core memory, a mixture of the two, or cache. MOS (metallic oxide semiconductor) memory uses industry standard 4K random access memory chips with a cycle time of 725 nanoseconds. MOS packaging provides up to 16K words on a single circuit board.

Optional battery backup is available to maintain MOS memory contents during a power failure.

8K or 16K words of core memory are provided on a single board, which mounts in one slot and overhangs the adjacent slot.

Parity memory, MOS or core, is standard on all PDP-11/34s, as is memory management and protection. This hardware feature is designed for systems where the memory size is greater than 28K words and for multi-programming systems where protection and relocation facilities are necessary.

Memory

Max size:	124K words
Type:	core or MOS
Parity:	standard

Cache Memory

The cache memory option utilizes a 2K byte direct mapping approach with an expected "hit" ratio of 86%. Detailed information on cache is presented in Chapter 8.

MOS

The basic unit of MOS memory, MS11-JP, contains 16K words of parity MOS memory. Each 16K words of MOS requires 1 hex mounting space.

Core

The basic unit of core memory, MM11-DP, contains 16K words of parity core memory. Each 16K words of core memory requires 2 hex mounting spaces.

Parity

All main memory in a PDP-11/34 system contains parity to enhance system integrity. Parity is generated and checked on all references between the CPU and memory, and any parity errors are flagged for resolution under program control. Odd parity is used, with one parity bit per 8-bit byte, for a total of 18 bits per word.

A double height module, M7850, contains parity control logic. Its control and status register (CSR) address is selectable between 772 100 and 772 136.

The CSR captures the high order address bits of a memory location with a parity error.

Battery Backup

Core memory is non-volatile; the contents are preserved when power is removed. However, MOS memory is volatile. If power is interrupted, an auxiliary power supply must be provided if information in the memory is to be saved. With the 5½" and 10½" CPU assemblies there is an optional battery backup unit that can preserve the contents of 32K words of MOS memory for about 2 hours. This auxiliary power unit is a battery that is charged up by the main AC power when the computer system is operating normally. In this normal mode, the battery backup has no effect on the MOS memory. But if power is interrupted, voltage-sensing circuitry within the backup option will automatically cause the MOS to be powered from this auxiliary power. The MOS information will be retained by being refreshed at a low cycle rate, using minimum power.

M9301 MODULE

The M9301 module, which is included with the PDP-11/34, provides four functions.

- It contains a read-only memory (ROM) that holds diagnostic routines for verifying computer operation.
- It contains, also in ROM, the several bootstrap loader programs for starting up the system.
- It contains the console emulator routine in ROM for issuing console commands from the terminal.
- It provides termination resistors for the UNIBUS.

There are two versions of the M9301 module available:

	M9301-YA	M9301-YB
Main user	OEM	End User
Able to run secondary bootstrap program directly upon power up or reboot	yes*	no
Automatic entry to console emulator routine	yes*	yes
Needs an ASCII terminal	no	yes

* Selection of one of these two operations is made by setting of switches contained on the module.

Diagnostics

Both versions of the M9301 contain diagnostics to check both the processor and memory in a Go/No-Go mode. Execution of the diagnostics occurs automatically but may be disabled by switches on the M9301.

Bootstrap Loader

The M9301-YA contains independent bootstrap programs that can bootstrap programs into memory from a selected peripheral device. Through front panel control or following power-up, the computer can execute a bootstrap directly, without the operator's keying in the initial program manually. The bootstrap program for the peripheral device is determined by switches on the M9301 board. This is especially useful in remote applications where no operator is present.

After execution of the CPU diagnostics, the M9301-YB turns control of the system over to the user at the console terminal. The system prints out status information and is ready to accept simple user commands for checking or modifying information within the computer, starting a program already in memory, or executing a device bootstrap.

The inclusion of a bootstrap loader in non-destructible read-only memory is a tremendous convenience in system operation. Bootstrap programs do not have to be loaded manually into the computer for system initialization.

Console Emulation

The normal console functions traditionally performed through front panel switches can be obtained by typing simple commands on the console terminal. LOAD, EXAMINE, DEPOSIT, START, and BOOT functions are available.

The M9301 module contains a console emulator routine. When this routine is used in conjunction with the terminal, functions quite similar to those found on the programmers' console of traditional PDP-11 family computers are generated.

Summary of the Console Emulator Functions

LOAD	Loads the address to be manipulated into the system.
EXAMINE	Allows the operator to examine the contents of the address that was loaded and/or deposited.
DEPOSIT	Allows the operator to write into the address that was loaded and/or examined.
START	Initializes the system and starts execution of the program at the address loaded.
BOOT	Allows the booting of a device specified by a 2-character code and optional unit number.

Console Emulator Operation

The console emulator allows the user to perform LOAD, EXAMINE, DEPOSIT, START, and BOOT functions by typing in the appropriate code on the keyboard.

Entry Into the Console Emulator

There are four ways of entering the console emulator:

- move the power switch to the ON position
- depress the BOOT switch
- automatic entry on return from a power failure
- load address manually

After the console emulator routine has started and the basic CPU diagnostics have all run successfully, a series of numbers representing the contents of R0, R4, SP, and PC will be printed by the terminal. This sequence will be followed by a $ on the next line.

Example — a typical printout on power up:

```
XXXXXX      XXXXXX      XXXXXX      XXXXXX
$
     R0          R4          R6          PC
                             STACK       PROGRAM
PROMPT                       POINTER     COUNTER
CHARACTER                    (SP)
```

NOTE: X signifies an octal numeral (0-7).

Whenever there is a power-up routine, or the BOOT switch is released from the INIT position, the PC at the time will be stored. The stored value is printed out as above (noted as the PC).

Detailed instructions about using the console emulator can be found in user instruction documents, the 11/34 *Users' Guide* and the associated hardware manuals.

Termination

The M9301 contains resistors for proper impedance termination at the end of the UNIBUS.

OPERATOR'S CONSOLE

The operator's console is the front panel link between the user and the computer. It contains a minimum number of switches and lights. All normally used console functions are available through the combination of the operator's console and an ASCII terminal, such as an LA36 DECwriter.

POWER	OFF	DC power to the computer is off.
	ON	Power is applied to the computer (and the system).
	STNBY	Standby; no DC power to the computer, but DC power is applied to MOS memory (to retain data). The fans remain on.
CONT/HALT	CONT	The program is allowed to continue.

	HALT	The program is stopped.
BOOT/INIT	INIT	The switch is spring-returned to the BOOT position. When the switch is depressed to INITialize and then return to BOOT, the operation depends on the setting of the CONT/HALT switch.
	HALT	Only the processor is initialized and no "UNIBUS INIT" is generated. Upon lifting the CONT/HALT switch, the M9301 routine is executed allowing examination of system peripherals without clearing their contents with "UNIBUS INIT."
	CONT	Initialize and then execute the M9301 program.

When the BOOT switch is released, the following action takes place:

A. For both M9301-YA and M9301-YB (when the switches are set for this operation):

1. Run basic CPU diagnostics.
2. Print out (on the console terminal) contents of R0, R4, SP, and PC at the time of power up, following by a dollar sign ($) on the next line.
3. Enter console emulator routine, awaiting keyboard commands.
4. When a device bootstrap command is issued, first run processor memory diagnostics, then execute secondary bootstrap program from the designated peripheral device.

B. For the M9301-YA (OEM) version only (when M9301-YA switches are set for this operation):

1. Run basic CPU diagnostics.
2. Run memory diagnostics.
3. Run secondary bootstrap program from the preselected peripheral device.

NOTE: When utilizing the stand-alone switch setting described as alternative b, above, the switches must be reset to enable execution of the console emulator routine.

PDP-11/34 PROCESSOR BACKPLANE CONFIGURATION

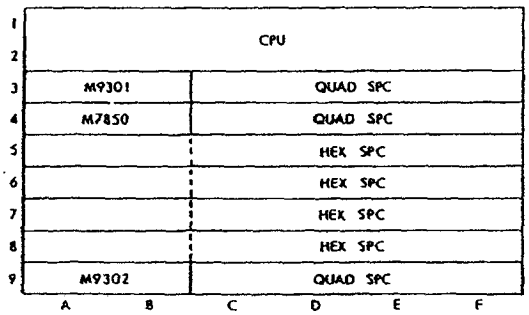
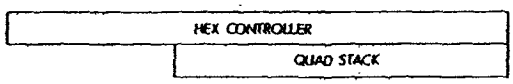


Figure 6-2 Processor Backplane

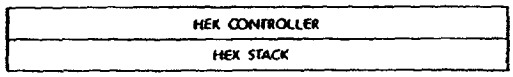
The processor backplane consists of a double system unit (SU) comprising 9 hex slots. All PDP-11/34 systems contain the CPU, M9301 Bootstrap/Terminator, M7850 parity control, and M9302 (or a UNIBUS jumper to the next SU) as shown in Figure 6-2. Memory is added as follows depending on whether the system uses core or MOS.

Core Memory:
Core memory is available in two size increments, 8K and 16K words.

The 8K core, MM11-C, consists of a hex and a quad module as follows:



The 16K core, designed MM11-D, consists of 2 hex modules as follows:



MOS Memory:
MOS memory is available in 8K or 16K increments and all increments consist of a single hex module.

8K and 16K increments are MS11-F and MS11-J.

The following backplane configurations constitute the basic PDP-11/34 computer.

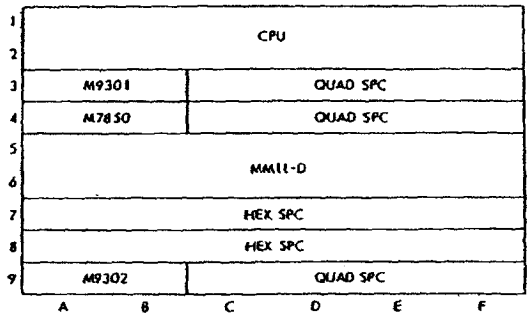


Figure 6-3 16K Core using MM11-D

Additional memory or quad and hex SPC options (DL11-W, TA11 controller, RX11 controller, etc.) may be added to the processor backplane as space allows.

MEMORY MANAGEMENT ON THE PDP-11/34

Memory Management and User Protection

The PDP-11/34's integral memory management facility allows a 16-bit machine to provide 18-bit capability for a four-fold extension of addressable memory. Access to memory is in as many as 32K units through eight programmable registers. These registers assign (or map) the virtual addresses, in 4K-word pages, to 4K-word physical

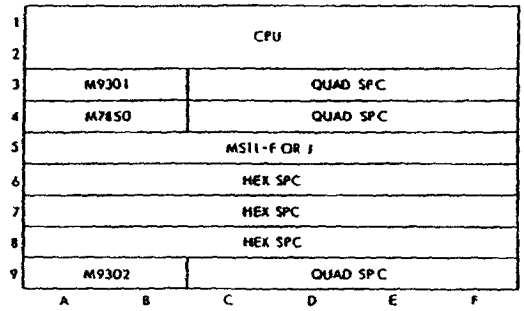


Figure 6-4 16K MOS using MS11-R or J

addresses anywhere within physical memory. The starting address of each 4K-word physical segment is stored in the registers.

Only virtual addresses need to be provided; transformation to physical addresses takes place automatically and transparently.

Programming

The memory management hardware has been optimized for a multi-programming environment. The processor can operate in two modes, **kernel** and **user**.

When in kernel mode, the program has complete control and can execute all instructions. Monitors and supervisory programs are executed in this mode.

When in user mode, the program is prevented from executing certain instructions that could:

- cause the modification of the kernel program
- halt the computer
- use memory space assigned to the kernel or to other users

In a multi-programming environment several user programs would be resident in memory at any given time. The task of the supervisory program would be to:

- Control the execution of the various user programs.
- Allocate memory and peripheral device resources.
- Safeguard the integrity of the system as a whole by careful control of each user program.

In a multi-programming system, the management unit assigns pages (relocatable memory segments) to your program and prevents you from making any unauthorized access to those pages outside your assigned area. Thus, you can effectively be prevented from accidental or willful destruction of any other user program or of the system executive program.

Hardware-implemented features enable the operating system to dynamically allocate memory upon demand, while a program is being run.

Basic Addressing

18-bit direct byte addresses are generated by PDP-11/34 and larger family members. Although the PDP-11 family word length is 16 bits, the UNIBUS and CPU addressing logic is actually 18 bits. Thus, while the PDP-11 word can contain address references only up to 32K words (64K bytes) the CPU and UNIBUS can reference addresses up to 128K words (256K bytes). These extra two bits of addressing logic provide the basic framework for expanding memory references.

In addition to the word length constraint on basic memory addressing space, the uppermost 4K words of address space are always reserved for UNIBUS I/O device registers. In a basic PDP-11 memory configuration (without management), all address references to the uppermost 4K words of 16-bit address space (160000-177777) are converted to full 18-bit references with bits 17 and 16 always set to 1. Thus, a 16-bit reference to the I/O device register at address 173224 is automatically converted internally to a full 18-bit reference to the register at address 773223. The basic PDP-11 configuration can then directly address up to 28K words of true memory and 4K words of UNIBUS I/O device registers, and, with memory-managed systems, 128K words.

Active Page Registers

The memory management unit uses two sets of eight 32-bit Active Page Registers (APR). An APR is actually a pair of 16-bit registers: a Page Address Register (PAR) and a Page Descriptor Register (PDR). These registers are always used as a pair and contain all the information needed to describe and relocate the currently active memory pages.

One set of APRs is used in kernel mode, and the other in user mode. The set to be used is determined by the current CPU mode contained in the processor status word.

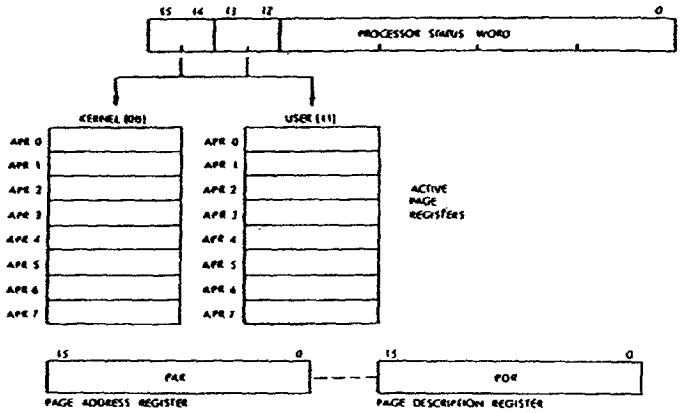


Figure 6-5 Active Page Registers

Capabilities Provided by Memory Management

Memory Size (words):	124K, max (plus 4K for I/O & registers)
Address Space:	Virtual (16 bits)
	Physical (18 bits)
Modes of Operation:	Kernel & User
Stack Pointers:	2 (one for each mode)
Memory Relocation:	
Number of Pages:	16 (8 for each mode)
Page Length:	32 to 4,096 words
Memory Protection:	no access
	read only
	read/write

Virtual Addressing

When the memory management unit is operating, the normal 16-bit direct byte address is no longer interpreted as a direct physical address (PA) but as a virtual address (VA) containing information to be used in constructing a new 18-bit physical address. The information

contained in the virtual address is combined with relocation and description information contained in the active page register to yield an 18-bit physical address.

Because addresses are relocated automatically, the computer may be considered to be operating in virtual address space. This means that no matter where a program is loaded into physical memory, it will not have to be re-linked; it always appears to be at the same virtual location in memory.

The virtual address space is divided into eight 4K-word pages. Each page is relocated separately. This is a useful feature in multi-progammmed timesharing systems. It permits a new large program to be loaded into discontinuous blocks of physical memory.

A basic function is to perform memory relocation and provide extended memory addressing capability for systems with more than 28K of physical memory. Two sets of page address registers are used to relocate virtual addresses to physical addresses in memory. These sets are used as hardware relocation registers that permit several users' programs, each starting at virtual address 0, to reside simultaneously in physical memory.

Program Relocation

The page address registers are used to determine the starting physical address of each relocated program in physical memory. Figure 6-6 shows a simplified example of the relocation concept.

Program A starting address 0 is relocated by a constant to provide physical address 6400_8.

If the next program virtual address is 2, the relocation constant will then cause physical address 6402_8, which is the second item of Program A, to be accessed. When Program B is running, the relocation constant is changed to 100000_8. Then Program B virtual addresses starting at 0 are relocated to access physical addresses starting at 100000_8. Using the active page address registers to provide relocation eliminates the need to re-link a program each time it is loaded into a different physical memory location. The program always appears to start at the same address.

A program is relocated in pages consisting of from 1 to 128 blocks. Each block is 32 words in length. Thus, the maximum length of a page is 4096 (128 X 32) words. Using all of the eight available active page registers in a set, a maximum program length of 32,768 words can be accommodated. Each of the eight pages can be relocated anywhere in the physical memory, as long as each relocated page begins on a

EXHIBIT 22

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EXHIBIT 23

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EXHIBIT 24

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EXHIBIT 25

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CERTIFICATE OF SERVICE

I, Julia Heaney, hereby certify that on May 31, 2006, I caused to be electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Paul M. Lukoff, Esquire
David E. Brand, Esquire
Prickett, Jones & Elliott, P.A.

and that I caused copies to be served upon the following in the manner indicated:

BY E-MAIL and BY HAND

Paul M. Lukoff, Esquire
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1310 King Street
Wilmington, DE 19899

BY E-MAIL and BY FEDERAL EXPRESS

Michael J. Summersgill, Esquire
Wilmer Cutler Pickering Hale and Dorr LLP
60 State Street
Boston, MA 02109

/s/ Julia Heaney
Julia Heaney (#3052)